UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/536,764	12/21/2005	Christian Paulus	I432.112.101/P29326	4668

45782 7590 08/21/2006

DICKE, BILLIG & CZAJA, PLLC
FIFTH STREET TOWERS
100 SOUTH FIFTH STREET
MINNEAPOLIS, MN 55402

EXAMINER	
NGUYEN, KHAI M	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 08/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/536,764	PAULUS, CHRISTIAN	
	Examiner	Art Unit	
	Khai M. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *41-45* is/are allowed.

6)☒ Claim(s) *24-26 and 46* is/are rejected.

7)☒ Claim(s) *27-40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/26/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. An initiated copy of the information disclosure statement (IDS) submitted on 5/26/2005 is attached herewith.

Specification

3. The application has not been checked to the extent necessary to determine the presence of all possible typographical and grammatical errors. However, Applicant's cooperation is requested in correcting any errors of which he/she may become aware in the application.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 24-26 and 46 are rejected under 35 U.S.C. 102(b) as being anticipated by Okada (US 5,798,725).

Regarding claim 24, Okada discloses an analog-to-digital converter (ADC 45 of Fig. 4; col. 5, lines 35-36) for converting a signal (VAi) to be digitized into a digitized signal (output of comparators 47A-C), comprising:

a plurality of comparators (CMOS inverters 56A-C and switches of Fig. 4 function as comparators), each of which has two inputs (coupled to switches S5-S6) and an output (nodes N7), wherein the output can be used to provide the digitized signal; and

an impedance network (switches S5-S8 of each comparator 47A-C) for each comparator, wherein each impedance network is connected between at least one input on the associated comparator (47A-C) and the signal to be digitized (VAi) and wherein each impedance network is connected between the associated comparator and a first electrical reference potential (VRH, VR2 or VRL),

wherein the impedance networks (switches S5-S8) are configured such that the comparators are brought essentially to the same operating point (col. 7, lines 47-64 – "...the voltages of the three nodes N6 and the output terminals (nodes N7) of the CMOS inverters 56A, 56B, and 56C are reset to the threshold voltage Vth").

Regarding claims 25-26, Okada discloses the ADC of claim 24, wherein the second input of at least some of the comparators (lowly CMOS inverters of Fig. 4) is brought to a second electrical reference or ground potential (the low-potential reference voltage VRL – col. 1, line 27)

Regarding claim 46, Okada discloses an integrated circuit (Fig. 4) including an analog-to-digital converter (ADC 45 of Fig. 4 – col. 4, lines 57-58), comprising:

a plurality of comparators (47A-C of Fig. 4) each having first and second inputs, which coupled to switches S5 & S6, and an output, which coupled to latch 49 of Fig. 4, wherein the output is configured to produce a digitized signal (at each output of the comparators); and

means (switches S5-S8 of Fig. 4) coupled to each comparator (i.e., the CMOS inverter 56A-C of the comparators) between at least one input of the associated comparator and a signal (VAi) to be digitized and between the associated comparator and a first electrical reference potential (VRH, VR2, VRL) for bringing the comparators to essentially the same operating point (col. 7, lines 47-64 – "...the voltages of the three nodes N6 and the output terminals (nodes N7) of the CMOS inverters 56A, 56B, and 56C are reset to the threshold voltage Vth").

Allowable Subject Matter

5. Claims 27-40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 41-45 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: for claims 27-40, the references of record neither reveal nor render obvious the recited limitations including the impedance networks as claimed.

For claims 41-45, the references of record also fail to teach or fairly suggest the recited combination including concepts of: using an impedance networks configured such that the comparators are brought to essentially the same operating point, splitting the signal to be digitized into a first signal part and a second signal part, and splitting the first electrical reference potential into a first potential part and a second potential part.

Prior Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclose (see references cited on PTO-892 Form attached herewith).

Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khai M. Nguyen whose telephone number is 571-272-1809. The examiner can normally be reached on 9:00 - 5:30 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford (Rex) Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Khai M. Nguyen
Art Unit: 2819

571-272-1809